ABSTRACT

There is provided an arithmetic circuit for minimizing the delay of data path from the input of data to be operated to the output of the result of operation of data. To that end, the arithmetic circuit comprises a first selector to which one input data and a fixed data are inputted wherein these data are selectively outputted in response to a control signal, a second selector to which another input data and an output data of a register are inputted wherein these data are selectively outputted in response to the control signal, an adder for receiving an output signal of the first selector and an output signal of the second selector to execute the addition of the output signals of the first and second selectors, and a register for receiving an output signal of the adder to hold the output signal in synchronization with a clock signal.